



Absolute encoders AFS/AFM60 SSI

AFM60A-TBAK262144



Model Name > [AFM60A-TBAK262144](#)
Part No. > [AFM60A-TBAK262144](#)



Illustration may differ

At a glance

- High-resolution absolute encoders with up to 30 bits (AFM60) or up to 18 bits (AFS60)
- Face mount flange, servo flange, blind or through hollow shaft
- SSI, SSI + Incremental or SSI + Sin/Cos interface
- Programmable resolution and offset (dependent on type)
- Connection system: M12, M23 connector or cable outlet
- Enclosure rating: IP 67 (housing), IP 65 (shaft)
- Operating temperature: -30 °C to +100 °C (depends on type)

Your benefits

- Programmability of the encoders means less storage, greater machine availability and easy installation
- Precise positioning due to high resolutions
- Large selection of mechanical interfaces and electrical contacting possibilities: Suitable for all applications
- Suitable for applications with limited space requirements (extremely short installation depth of 30 mm)
- Very good rotation accuracy due to increased bearing distance
- One programming tool and software with automatic encoder detection for AFS60/AFM60/DFS60



Performance

Max. number of steps per revolution:	262,144
Max. number of revolutions:	4,096
Resolution power:	262,144 x 4,096
Resolution:	18 bit x 12 bit
Error limits:	± 0.03 °
Repeatability (Ta not constant):	0.002 °
Measuring step deviation:	± 0.002 °
Measuring step:	0.014 °
Initialization time:	50 ms ¹⁾

¹⁾ Valid positional data can be read once this time has elapsed

Mechanical data

Mechanical interface:	Through hollow shaft
Shaft diameter:	8 mm

Start up torque:	0.8 Ncm (20 °C)
Operating torque:	0.6 Ncm (20 °C)
Maximum operating speed:	9,000 /min ¹⁾
Moment of inertia of the rotor:	40 gcm ²
Bearing lifetime:	3.0 x 10 ⁹ revolutions
Max. angular acceleration:	500,000 rad/s ²
Permissible movement axial static/dynamic:	± 0.5 mm, ± 0.01 mm
Permissible movement radial static/dynamic:	± 0.3 mm, ± 0.05 mm

¹⁾ Self warming of 3.3 K per 1000 revolutions/min when applying note working temperature range

Electrical data

Power consumption:	0.5 W (without load)
Operating voltage range:	4.5 V DC ... 32 V DC
MTTFd: mean time to dangerous failure:	250 a (EN ISO 13849-1) ¹⁾

¹⁾ This product is a standard product and does not constitute a safety component as defined in the Machinery Directive.

Calculation based on nominal load of components, average ambient temperature 40°C, frequency of use 8760 h/a. All

electronic failures are considered hazardous. For more information, see document no. 8015532.

Interfaces

Electrical interface:	Cable, 8-pin, universal, 1.5 m ¹⁾
Interface signals:	Clock +, Clock -, Data +, Data- ²⁾
Clock frequency:	2 MHz
SET (electronic adjustment):	H-active (L ≡ 0 - 1,5 V, H ≡ 2,0 - Us V)
CW/CCW (counting sequence when turning):	L-active (L ≡ 0 - 1,5 V, H ≡ 2,0 - Us V)

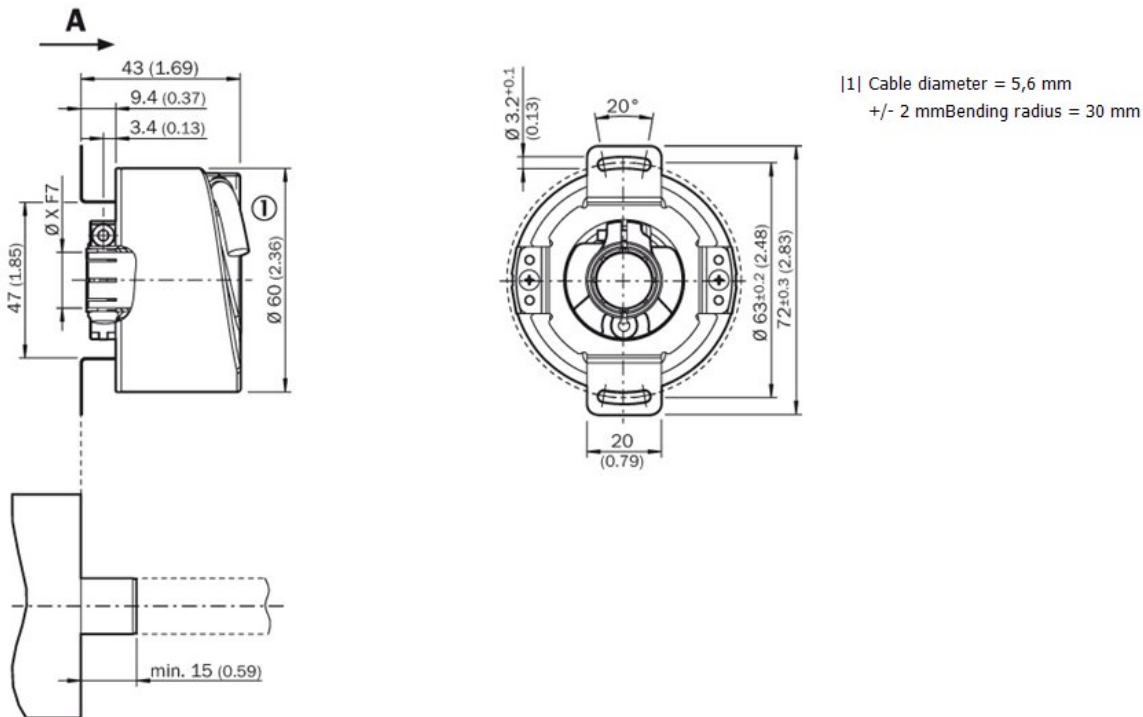
¹⁾ The universal cable outlet is positioned in such a way, that it is possible to lay the cable in a radial or axial direction without kinking it ²⁾

Ambient data

EMC:	(according to EN 61000-6-2 and EN 61000-6-3) ¹⁾
Enclosure rating:	IP 65 (according to IEC 60529), IP 65 (according to IEC 60529), shaft side
Permissible relative humidity:	90 % (condensation of the optical scanning not permitted)
Working temperature range:	-30 °C ... 100 °C
Storage temperature range:	-40 °C ... 100 °C, without package
Resistance to shocks:	60 g (according to EN 60068-2-27)
Resistance to vibration:	20 g, 10 Hz ... 2,000 Hz (according to EN 60068-2-6)

¹⁾

Dimensional drawing



Signalausgänge

SSI data format singleturn



Bit 1-18: Position Bits

- LSB: Least significant Bit
- MSB: Most significant Bit

Bit 19-21: Error Bits

- ERRDIG: Failure message about speed. If this failure occurs during the position building procedure it will be indicated by the ERRDIG-Bit.
- ERRSL: Light source monitoring failure.
- ERRSYNC: Contamination of the disc or scanning system. During the determination of the position, an error has occurred since the last SSI transmission. The error bit will be deleted during the next data transmission.

The evaluation of the error bits has to be realized in the PLC.

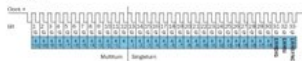
The provided error bits don't have to be used by the PLC compulsorily.

Example

If the resolution of the absolute encoder is set on 13 bits, 16 bits are provided by the encoder: 13 data bits and 3 error bits. If the PLC is not able to evaluate the error bits, the PLC has to be set on a resolution of 13 bits. Then the error bits have to be masked out by the PLC.

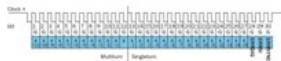
SSI data format multiturn

30 Bits



- Bit 1-12: Position Bits multiturn
- Bit 13-30: Position Bits singleturn
- Bit 31-33: Error Bits

27 Bits



- Bit 1-12: Position Bits multiturn
- Bit 13-27: Position Bits singleturn
- Bit 28-30: Error Bits

Error Bits

- ERRDIG: Failure message about speed. If this failure occurs during the position building procedure it will be indicated by the ERRDIG-Bit.
- ERRSL: Light source monitoring failure.
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The evaluation of the error bits has to be realized in the PLC.

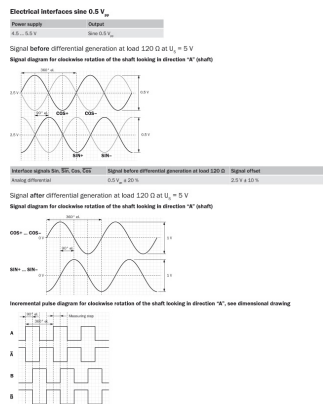
The provided error bits don't have to be used by the PLC compulsorily. The multiturn resolution is fixed on 12 bits.

Example

If the resolution of the absolute encoder is set on 27 bits, 30 bits are provided by the encoder: 27 data bits and 3 error bits. If the PLC is not able to evaluate the error bits, the PLC has to be set on a resolution of 27 bits. Then the error bits have to be masked out by the PLC.

The graph illustrates the relationship between the speed of the motor (N in min^{-1}) and the number of steps per revolution. The y-axis, labeled 'Steps per revolution', ranges from 16,384 to 262,144. The x-axis, labeled 'Speed N [min^{-1}]', ranges from 0 to 12,000. The curve shows a sharp decrease in steps per revolution as speed increases, eventually leveling off at a constant value of 16,384 steps per revolution for speeds above approximately 8,000 min^{-1} .

Interfaces



SSI data format multibit error

The diagram illustrates the timing of an SSI data format multibit error. It shows a sequence of 16 clock cycles. In cycle 1, a 'Data Error' occurs. The error is detected in cycle 2, where the error signal is high. The error is then propagated through the system, with the error signal remaining high for 16 clock cycles. The error is then cleared in cycle 17, where the error signal is low. The diagram also shows the timing of the error signal relative to the data and clock signals.

Bit 1 - 16: Position Bits

- **ERR0:** Light source monitoring bit
- **ERR1:** Light source alignment bit
- **ERR2:** Error signal

Bit 17 - 23: Error Bits

- **ERR3:** Error signal
- **ERR4:** Error signal
- **ERR5:** Error signal
- **ERR6:** Error signal
- **ERR7:** Error signal
- **ERR8:** Error signal
- **ERR9:** Error signal
- **ERR10:** Error signal
- **ERR11:** Error signal
- **ERR12:** Error signal
- **ERR13:** Error signal
- **ERR14:** Error signal
- **ERR15:** Error signal
- **ERR16:** Error signal
- **ERR17:** Error signal
- **ERR18:** Error signal
- **ERR19:** Error signal
- **ERR20:** Error signal
- **ERR21:** Error signal
- **ERR22:** Error signal
- **ERR23:** Error signal

Timing of the error bits to be read in the PLE

The error bits of the error bits to be read in the PLE completely. The multibit error is read in 16 clock cycles.

Example:

If the multibit error of the absolute encoder is set to 17 bits, 16 bits are provided by the encoder: 13 data bits and 3 error bits. The error bit is not available in the error bits, the PLE has to set a reservation of 13 bits. Then the error bits have to be read in the PLE.

SSI data format multibit error

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Bit 1 - 16: Position Bits

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Bit 17 - 23: Error Bits

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- **ERR4:** Error signal
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- **ERR6:** Error signal
- **ERR7:** Error signal
- **ERR8:** Error signal
- **ERR9:** Error signal
- **ERR10:** Error signal
- **ERR11:** Error signal
- **ERR12:** Error signal
- **ERR13:** Error signal
- **ERR14:** Error signal
- **ERR15:** Error signal
- **ERR16:** Error signal
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- **ERR18:** Error signal
- **ERR19:** Error signal
- **ERR20:** Error signal
- **ERR21:** Error signal
- **ERR22:** Error signal
- **ERR23:** Error signal

Timing of the error bits to be read in the PLE

The error bits of the error bits to be read in the PLE completely. The multibit error is read in 16 clock cycles.

Example:

If the multibit error of the absolute encoder is set to 27 bits, 26 bits are provided by the encoder: 27 data bits and 2 error bits. The error bit is not available in the error bits, the PLE has to set a reservation of 27 bits. Then the error bits have to be read in the PLE.

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